# ULTRA LOW POWER HFET DOWN CONVERTER FOR WIRELESS COMMUNICATION APPLICATIONS

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## Abstract

An ultra low power GaAs HFET (heterojunction FET) amplifier/mixer MMIC was designed and characterized for portable communication applications in the 900 MHz band. A completely monolithic LNA (80 mil X 42 mil) achieved 10 dB gain, 2.5 dB NF and -4 dBm input IP3 at an operating current of 0.5mA @ 1.0 V. A down converter, consisting of the LNA and a dual gate FET mixer achieved -117 dBm receiver sensitivity in the 900 MHz cellular band. The total power consumption of this miniature down converter was about 2 mW. The HFET down converter IC achieved the same receiver sensitivity as a MESFET down converter at 1/5$^{th}$ of the power. The extremely low power dissipation, high third order intercept point, high level of integration, and very good RF performance of this monolithic IC make it an ideal candidate for wireless applications.

## Introduction

GaAs MMIC receivers in wireless communication products lead to a reduction in the number of parts and interconnects and, hence, the size and weight. However, to conserve the battery drain in portable units, devices and circuits have to be designed to operate at very low current levels. Enhancement mode and depletion mode MESFET MMIC amplifiers with excellent RF performance at low current levels have been published(1-6). This paper reports on the development of an GaAs HFET MMIC down converter with low power dissipation for wireless communication applications.

## Circuit Design

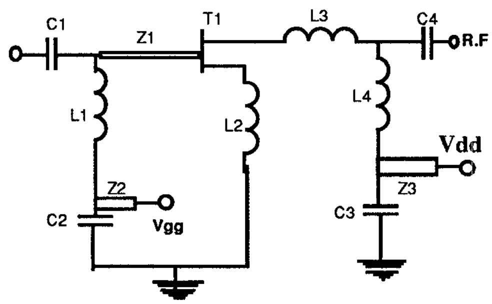


**Fig. 1a. LNA MMIC schematic**

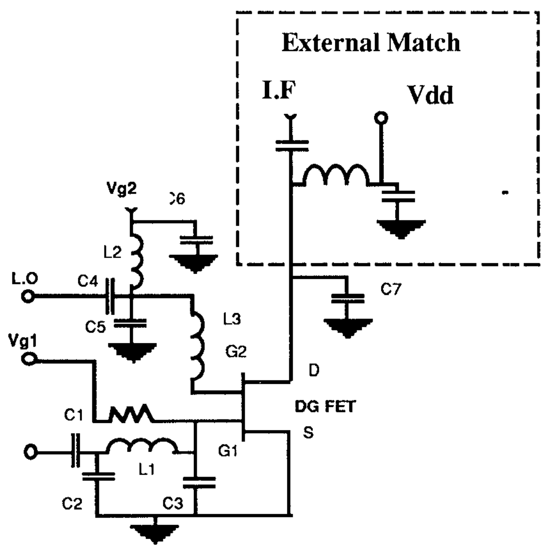


**Fig. 1b. Dual gate FET mixer schematic**





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The design goal was to demonstrate a low power integrated front-end technology for wireless applications. Improving the intermodulation characteristics of the low power amplifier was also an important goal. A down converter operating at 1.0 V with less than 2 mA operating current was chosen as the demonstration vehicle. It consisted of a single stage GaAs HFET low noise amplifier(LNA) and a dual gate FET mixer as shown in fig. 1a and 1b. A lumped element LC matching network was employed in the design to achieve on-chip selectivity. The noise parameters of the HFET were measured at very low current levels using an internally developed measurement system. Single stage amplifiers were modelled with different gate width devices were to study the IP3-gain-NF-return loss tradeoff. In order to improve the input third order intercept point of low power LNAs, device harmonics were measured at low frequencies(7). The circuit IP3 was modeled by representing the device nonlinearities in Volterra series(8). The circuit was optimized to give high IP3, good frequency response, and good return loss, while maintaining unconditional stability.

## Results and Discussion

The wafers were fabricated using a 0.7 μm GaAs HFET MMIC process developed in-house. This process employs epitaxial material with InGaAs channel, and AlGaAs planar doped barriers, Ni/Ge/Au ohmics, Ti/Al Schottky gate and two level metal interconnects. Figure 2 shows the maximum gain comparison between the nominal 0.7 μm gate length HFET and MESFETs as a function of drain current at 2 GHz. For MMIC fabrication, on-chip $Si_3N_4$ MIM capacitors and 3μm thick Au inductors were employed. The fabricated LNA chip, and the mixer chip are shown in figs. 3a and 3b.

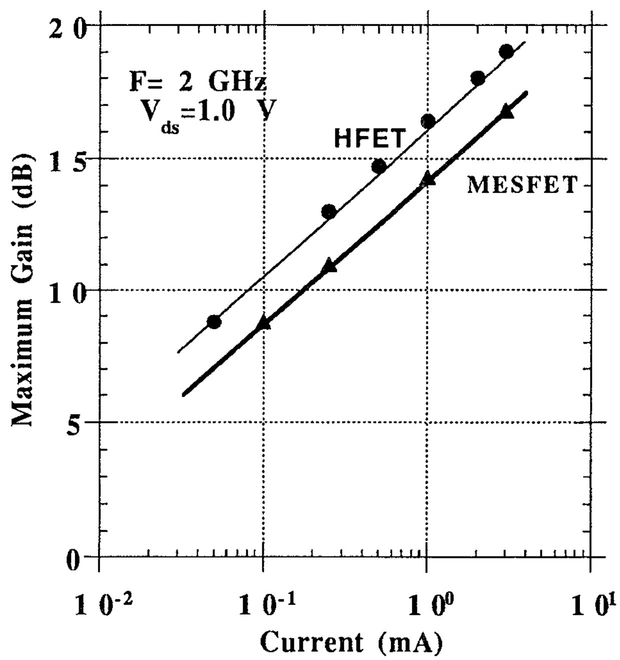


Fig. 2 Maximum Gain of a MESFET & HFET Device size= 0.7 μm X 50 μm

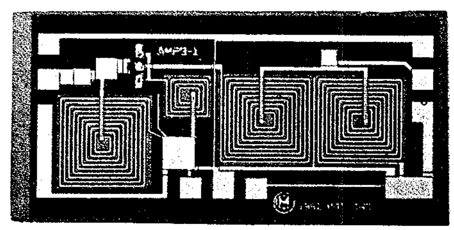

Fig. 3a. Fabricated LNA MMIC chip

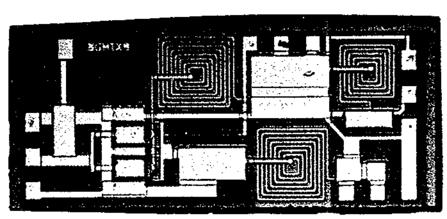

Fig. 3b. Fabricated DG FET Mixer chip

## Amplifier

The amplifier consists of a 100 µm HFET with on-chip input and output matching. The gain, IP3, return loss and noise figure were measured on-wafer using an integrated test system developed in-house. The measured gain, IP3 and noise figure of the amplifier are plotted in fig. 4. This amplifier achieved a gain of 10 dB and noise figure of 2.5 dB at operating current of 0.5 mA and 1.0V supply voltage. At this low bias point, the amplifier also exhibited very high input IP3 of -4.0 dBm. In fig. 5, this amplifier performance is compared with published results of other MMIC LNAs. To our knowledge, this MMIC amplifier is the lowest power consumption amplifier reported to date.

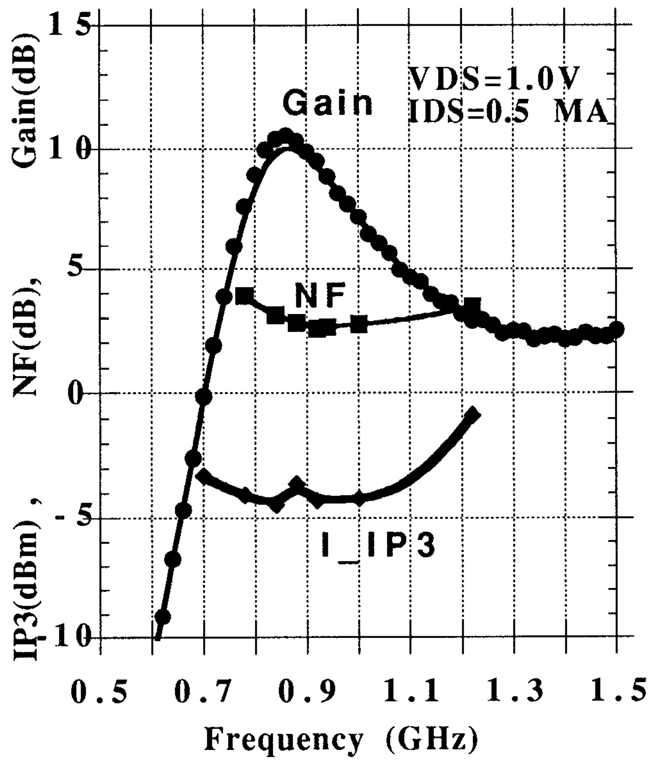


**Fig. 4 Measured performance for MMIC LNA Vds= 1.0V, Ids= 0.5 mA**

## Mixer

A dual gate HFET mixer design was accomplished by using a cascoded connection of two single gate HFETs. RF and L.O. ports were matched on-chip, while the IF port was matched externally to the chip.

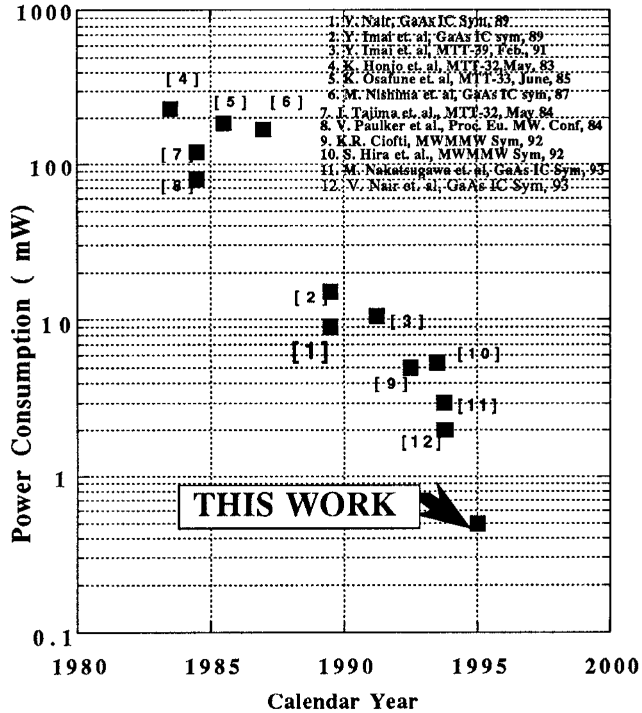


**Fig. 5.MMIC LNA power consumption (LNAs with on-chip matching and Gain ≥ 10 dB are included)**

This monolithic mixer achieved a conversion gain of -0.2 dB and intercept point of + 1 dBm at 1.0 mA. Mixer performance showed a strong dependence on the voltage applied to the second gate. The optimized second gate voltage was used in the down converter test described below.

## Down Converter IC

In order to evaluate the performance of the HFET LNA and mixer IC, the wafers were thinned, scribed and assembled in the 14 pin SOIC and ceramic packages. A complete receiver system was built using the HFET LNA and mixer IC cascaded with a narrow band FM double conversion receiver IC (MC3363DW) and an audio amplifier (MC34119D). The receiver sensitivity of the HFET down converter was measured using a SINAD(SIgnal, Noise And Distortion) measurement system (9). 12 dB SINAD is a specified standard for sensitivity measurement of professional radio receivers such as land mobile and cellular radios. The measured performance of the down converter IC is shown in fig. 6. HFET MMIC down converter achieved -117 dBm receiver sensitivity at 2 mW of power. This is an 80% reduction in power consumption compared to a MESFET down converter (9).

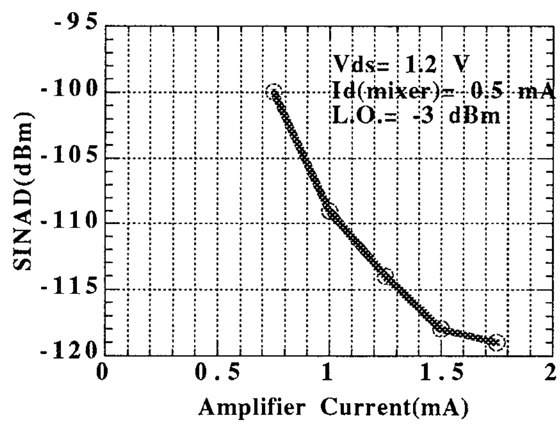


**Fig 6. HFET down converter sensitivity at cellular band**

## Conclusion

A fully monolithic GaAs HFET MMIC amplifier and mixer was designed, fabricated and tested for potential application in wireless communication system. The total power dissipation of the miniaturized IC was only 2mW. This single chip integrated front-end IC (80 mil X 85 mil) achieved -117 dBm sensitivity in the 900 MHz cellular band. The HFET down converter IC achieved same receiver sensitivity as a MESFET down converter at 1/5$^{th}$ of the power. The extremely low power dissipation, high level of integration and very good RF performance of this monolithic IC make it an ideal candidate for portable communication applications.

## Acknowledgements

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